Eng. Guerino Mangiamele (Member of EMA)

H.B University

Architettura dei sistemi a microprocessori

Breve introduzione ai Microprocessori INTEL e Motorola   Parte 1

_____

Microprocessors Architecture

A brief History of INTEL and Motorola Microprocessors Part 1

Abstract

I primi Microprocessori INTEL

Il primo microprocessore ad appararire sul mercato fu l'INTEL 4040 , un dispositivo con 4 bit di dati . Questo, a distanza di un paio di anni , fu seguito dall'8008 , con bus a 8 bit . Successivamente, altri due microprocessori a 8 bit (8080 e 8085) furono introdotti sul mercato a metà degli anni 70 - Questi due dispositivi potevano indirizzare solo 216 locazioni di memoria ….

I primi microprocessori MOTOROLA

Il primo microprocessore della Motorola fu un dispositivo a 8 bit (8 bit di bus di dati). Il 6800 fu immesso sul mercato nel 1975 , aveva una frequenza di clock di 2 MHz ed era in grado di indirizzare 64 Kbytes di memoria con 16 bit di bus indirizzi . Nel 6802 , furono implementate 128 Kbytes di RAM da usare come registri . Nel 6803 la frequenza di clock fu incrementata a 3.58 MHz e fu aggiunta una UART (Universal Asynchronous Receiver/transmitter) per le comunicazioni seriali . L'ultimo dei microprocessori a 8 bit fu il 6809 che includeva un set di istruzioni avanzato . Tutti i dispositivi a 8 bit possedevano un bus indirizzi a 16 bit …

The Early Intel Microprocessors

The first microprocessor to appear in the market was the Intel **4004**, a 4-bit data bus device. This device was followed by the **8008**, which had an 8-bit data bus.

Two more 8-bit microprocessors (reference to the number of bits usually refers to the data bus unless stated otherwise), the **8080** and **8085** were introduced in the mid-1970s. These two devices could address only 216 memory locations.

The 80X86 Family of Microprocessors

Since its introduction in 1978, the so-called X86 architecture has undergo five major evolutionary stages. The term *architecture* in relation to microprocessors refers to the internal design and organization of the device.

The first generation of the 80X86 family includes the **8086**, the **8088**, and the **80186**. Next, came the **80286**, followed by the **80386**, and then the **80486**. The **Pentium** is the fifth generation Intel microprocessor. Each generation built upon the basic concept of the first additional features and improved performance.

Intel 8086/8088 and 80186

!"Introduced in 1978, the **8086** was the first 80X86 family and is the basis for all Intel microprocessors that followed.

!"The 8086 was a 16-bit microprocessor (16-bit data bus) and represented a significant departure from the earlier 8-bit devices.

!"Owned 20 address lines (allowing 220 memory locations to be accessed).

!"The various versions of the 8086 operated at clock frequencies of %, 8, or 10MHz.

!"The **8088** is essentially an 8086 with the 16-bit internal data bus multiplexed down to an 8-bit external bus. It was intended to meet the demand for applications in simpler 8-bit systems and was used in the original IBM personal computer (PC).

!"The **80186** is an 8086 with several support functions such as clock generator, system controller, interrupt controller, and direct memory access (DMA) controller integrated on the chip. An increased clock frequency of 12.5MHz was added and the 5MHz available in the 8086/8088 was dropped, resulting in a selection of 8, 10, or 12.5MHz.

Intel 80286
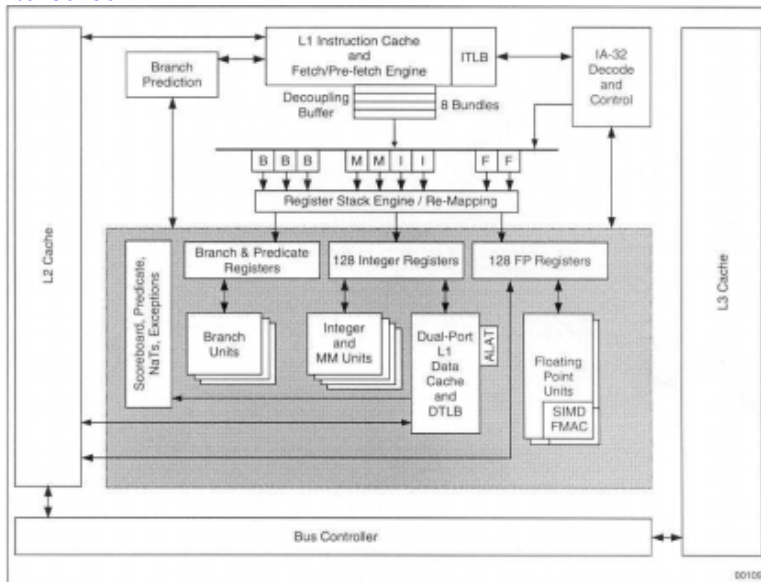
! "Introduced in 1982, the memory addressing capability was increased to 24 address lines.

!"First Intel processor to include an advanced mode of operation (used in the next generations of microprocessors): *protected mode*. This mode allows access to additional memory locations and advanced programming features.

!"It operates at the same clock frequencies as the 80186.

Intel 80386

!"Introduced in 1985, it was the first 32-bit Intel microprocessor (32-bit data bus + 32-bit address bus).

!"The first Intel microprocessor to use instruction pipelining.

!"All 80386 versions can operate in conjunction with math (floating-point) co-processors.
!"More economical versions: 80386SX and 80386SL, in which the data bus is multiplexed down to 16 bits and the address bus down to 24 bits.
!"Versions that operate at clock frequencies of 16, 20, 25 and 33MHz are available.

Intel 80486
!"Introduced in 1989, it incorporates an 8Kbytes cache memory (shared for data and instruction).
!"The first Intel processor to present an internal floating point unit (FPU).
!"Different versions operate at clock frequencies from 25 to 100MHz (Intel 80486 DX4).

Pentium
!"Introduced in 1993, retains the 32-bit address bus of the 80486 but doubles the data bus to 64 bits.
!"Presents two 8Kbytes cache memories (one for instruction, one for data).
!"Dual pipeline method, known as superscalar architecture.

The Early Motorola Microprocessors

The first microprocessors from Motorola were all 8-bit devices (8-bit data bus). The **6800** appeared in 1975 with a clock frequency of 2MHz and capable of addressing 64 Kbytes of memory with a 16-bit address bus.
In the **6802**, a 128Kbytes RAM was added for use in the place of some registers. The clock frequency was increased in the **6803** to 3.58MHz, and a UART (Universal Asynchronous Receiver/Transmitter) was added for serial communications.
The last of the 8-bit microprocessors was the **6809** which offered an enhanced instruction set including a multiply instruction.
All of the 8-bit devices retained the 16-bit address bus.

The 680X0 Family of microprocessors
The Motorola 680X0 family of microprocessors is split into five generations. It was started in 1978, with the MC68000, and was concluded in 1994 with the MC68060. The PowerPC family is the sixth generation of Motorola microprocessors.

Motorola 68000
!"Introduced in 1978.
!"The RAM-based register concept used in some of the 8-bit devices was abandoned in favor of 16 general-purpose registers.
!"The industry's lowest cost 32-bit microprocessor.
!"The **MC68HC000** is a CMOS version of the original MC68000. The MC68EC000 version provides a lower cost 68000 solution. The **MC68SEC000** version provides a static, low power implementation consuming only 15.0mA in normal 3.3V operation and 0.5mA in static standby mode.
!"32 Bit Data and Address Registers.
!"24 address lines. 16 Mbytes Direct Addressing Range.
!"56 Powerful Instructions. 14 Addressing Modes.
!"2 MIPS at 20MHz.
!"Available in 8, 10, 12, 16 & 20 MHz speeds.

PowerPC 601/601v

!"*The PowerPC 601/601v Microprocessor:* The PowerPC 601 microprocessor is the first 32-bit implementation of the PowerPC Reduced Instruction Set Computer (RISC) architecture. The PowerPC 601 microprocessor provides high levels of performance for desktop, workstation,and symmetric multiprocessing computer systems and offers design flexibility through operation at either 2.5 volts (601v) or 3.6 volts (601).

!"*Superscalar Microprocessor:* The PowerPC 601 microprocessor is a superscalar design capable of issuing and retiring three instructions per clock. Instructions issue to multiple execution units, execute in parallel, and can complete out of order, while preserving program correctness. The PowerPC 601 integrates three execution units: an integer unit (IU), a branch processing unit (BPU), and a floating-point unit (FPU). It also incorporates a memory management unit (MMU), a unified instruction and data cache, a real-time clock (RTC), and on-chip test capability. The ability to execute multiple instructions in parallel and the use of simple instructions with rapid execution times yield maximum efficiency and throughput for PowerPC systems.

!"*Cache and MMU Support:* The PowerPC 601 microprocessor includes an on-chip, 32-Kbyte, eight-way set-associative, physically addressed, unified (instruction and data) cache.
An on-chip MMU contains 256-entry, two-way set-associative, unified (instruction and data) translation lookaside buffer (UTLB) and provides support for demand paged virtual memory address translation and variable-sized block translation.

!"*Flexible Bus Interface:* The PowerPC 601 microprocessor has a high bandwidth, 64-bit data bus and a separate 32-bit address bus. The interface protocol allows multiple masters to access system resources through a central external arbiter. Additionally, on-chip snooping logic maintains cache coherency in multiprocessor applications.

PowerPC 601 Major Features:

Specifications Summary

- !"32-Kbyte unified cache
- !"Superscalar-3 instructions per clock
- !"Multiple execution
- !"64-bit data bus
- !"L2 cache
- !"*Power consumption:* Full operation - 10 watts maximum at 80 MHz

Technology

- !"3.6-volt implementation
- !"0.6-micron static CMOS technology
- !"120 mm2 die size
- !"2.8 million transistors Packaging
- !"304 CQFP

PowerPC 601v Major Features:

Specifications Summary

- !"32-Kbyte unified cache

- !"Superscalar-3 instructions per clock
- !"Multiple execution
- !"64-bit data bus
- !"L2 cache
- !"*Power consumption:* Full operation - 6 watts maximum at 100 MHz

Technology
- !"2.5-volt implementation with 5-volt I/O
- !"0.5-micron static CMOS technology
- !"74 mm2 die size
- !"2.8 million transistors
- !"304 CQFP

MOTOROLA PowerPC MPC7450

!"The **MPC7450 PowerPC** microprocessor is a high-performance, low-power, 32-bit implementation of the PowerPC RISC architecture with a full **128-bit implementation** of Motorola's **AltiVec technology**. This microprocessor is ideal for leading edge computing, embedded network control, and signal processing applications. The MPC7450 has a new, deeper, **seven-stage pipeline with two additional execution units**. The **L2 cache has been integrated onto the die** for greater speed, and supports a **large backside L3 cache** with a **64-bit datapath**. The MPC7450 offers increased address space and high-bandwidth
MPX bus with minimized signal setup times and reduced idle cycles to increase bus bandwidth to a maximum speed of **133 MHz**. MPC7450 processors offer single-cycle throughput **double precision floating-point performance** and full symmetric multiprocessing (**SMP**) capabilities. Finally, the MPC7450 is software-compatible with existing PowerPC 603e, 750, 7400 and 7410 processors and exploits the full potential of AltiVec technology.

!"The MPC7440 PowerPC processor is a low-power version of the high performance MPC7450.
This microprocessor is a small, 360-pin package that does not include the backside L3 cache. It has a core voltage of 1.5 V and is available at speeds of 600 and 700 MHz.
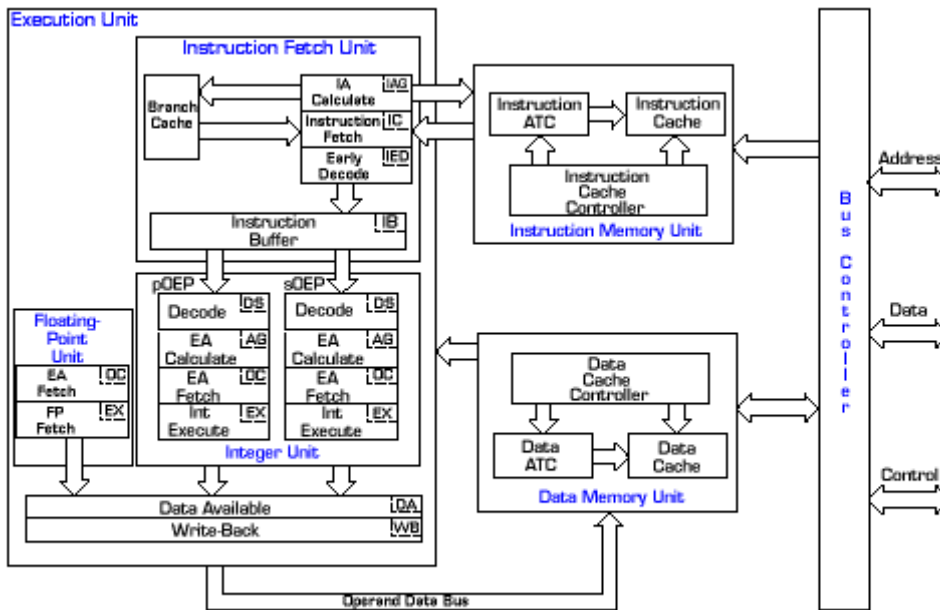
!"*Superscalar Microprocessor:* MPC7450 microprocessors feature a high-frequency superscalar PowerPC core, capable of issuing four instructions per clock cycle (three instructions + branch) into eleven independent execution units:

- Four integer units (3 simple + 1 complex)
- Double-precision floating-point unit
- Four AltiVec units (simple, complex, floating, and permute)
- Load/store unit
- Branch processing unit

!"*Cache and MMU Support:* The MPC7450 microprocessor has separate 32KB, physically addressed instruction and data caches. Both L1 caches feature cache way locking and are eight-way set associative. For greater speed, the L2 cache has been integrated on-chip with a 256-bit interface to L1 which operates at processor frequency. This L2 is 256KB eight-way set associative. L2 cache access is fully pipelined. The MPC7450 also supports

an L3 cache interface with on-chip tags to support up to 2MB of off-chip cache.

The L3 data bus is 64-bits wide, provides multiple SRAM options, and affords critical quad-word forwarding to reduce latency. The off-chip L3 storage can also be configured as a local addressable memory. Finally, in addition to supporting hardware table searching on a TLB miss, the MPC7450 can be configured for software table searching. In this case, TLB entries are loaded by the system software. The MPC7450 microprocessor contains separate memory management units for instructions and data, supporting 4 Petabytes (252) of virtual memory and up to 64 Gigabytes (236) of physical memory. The MPC7450 also has four-

instruction block address translation and four data block address translation registers.

!"*MPX Bus Interface:* MPC7450 microprocessors support the MPX bus protocol with a **64-bit data bus** and a **32- or 36-bit address bus**. Support is included for **burst**, **split**, **pipelined** and **out-of-order transactions**, in addition to **data streaming**, and **data intervention** (in SMP systems). The interface provides **snooping for data cache coherency**. The MPC7450 implements the **cache coherency protocol for multiprocessing support in hardware**, allowing access to system memory for additional caching bus masters, such as DMA devices.

!"*Power Management:* MPC7450 microprocessors feature a low-power 1.8-volt design with **three power-saving user-programmable modes** (**nap**, **doze** (with bus snoop) and **sleep**) which progressively reduce the power drawn by the processor. The MPC7450 also provides a **thermal assist unit** and **instruction cache throttling** for **software-controllable thermal management**.
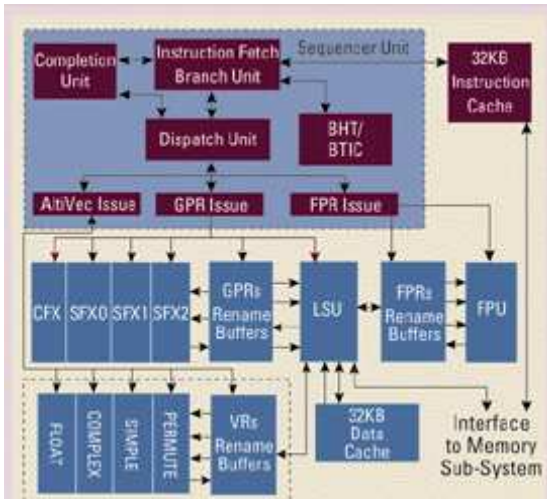
AltiVec Technology: The AltiVec technology expands the capabilities of Motorola's fourth generation PowerPC microprocessors by providing leading-edge, general purpose processing performance while concurrently addressing high-bandwidth data processing and algorithmic-intensive computations in a single-chip solution.

 AltiVec technology:
Meets the computational demands of networking infrastructure such as echo cancellation equipment, and base station processing.
Enables faster, more secure encryption methods optimized for the SIMD processing model.
Provides compelling performance for multimedia-oriented desktop computers, desktop publishing, and digital video processing.
Enables real-time processing of the most demanding data streams (MPEG-2 encode, continuous speech recognition, real-time high resolution 3D memory for 3D graphics.)

Next : part2   A microprocessor equipment in a control lines system

Ing. Guerino Mangiamele
Enertec Research R&S
Ricerca e Sviluppo
gmangiamele@enertec.org